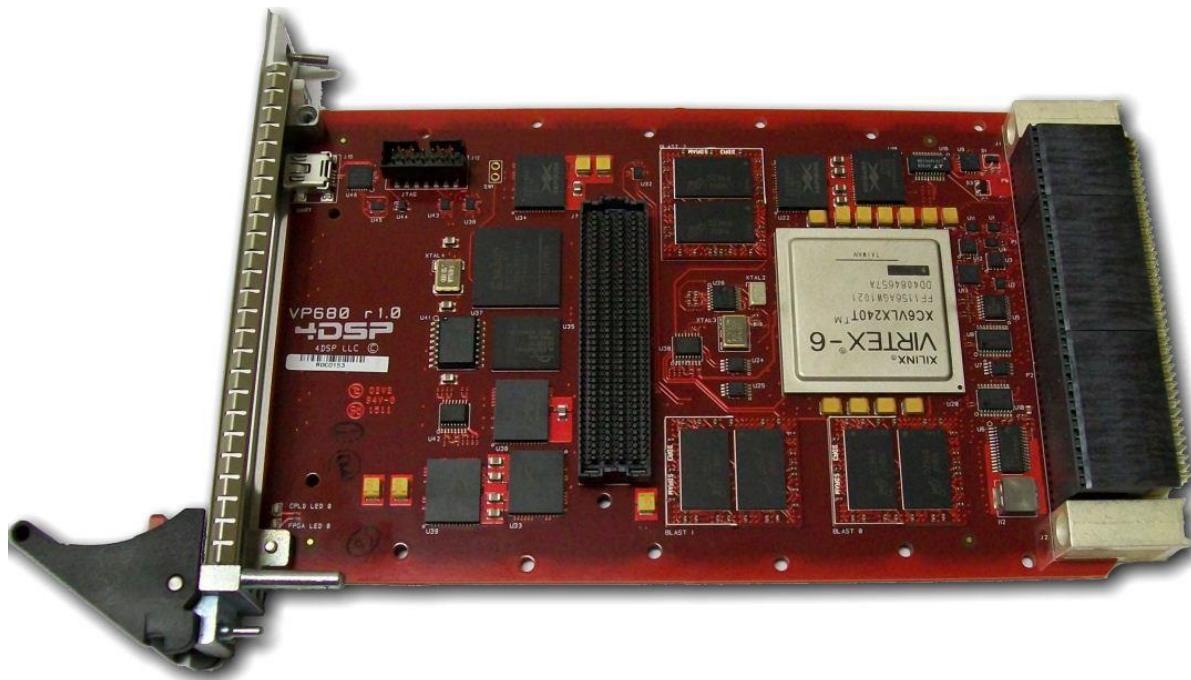


# VP680

## User Manual



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## Revision History

Date	Revision	Revision
2011-03-23	Draft	0.1
2011-05-11	Added FPGA pin out tables. Textual changes. Internally reviewed.	0.2
2011-05-12	Added direction information on peripheral pins. Added FLASH and configuration info. Added BLAST VIO matrix.	0.3
2011-05-12	Release	1.0
2011-05-13	Added product photo. Update errata appendix.	1.1
2011-08-01	Correction of commercial temperature range.	1.2
2011-09-09	Added OpenVPX profile specification. Added weight specification.	1.3
2014-08-21	Added description to section 3.1.2 about a mechanical exception made to the VITA 48.2 standard with regards to the clamshell. Added conduction-cooled clamshell drawing.	1.4
2015-06-22	Added detail to power supply section, replaced references to Virtex5 with Virtex6	1.5

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## 1 Acronyms and related documents

### 1.1 Acronyms

A/D	Analog to Digital Converter
BLAST	Board Level Advanced Scalable Technology
CPLD	Complex Programmable Logic Device
D/A	Digital to Analog Converter
DCI	Digitally Controlled Impedance
DDR	Double Data Rate
DSP	Digital Signal Processing
FBGA	Fineline Ball Grid Array
FFT	Fast Fourier Transformation
FMC	FPGA Mezzanine Card
FPDP	Front Panel Data Port
FPGA	Field Programmable Gate Array
GPIO	General Purpose Input/Output
GUI	Graphical User Interface
HPC	High pin count
IP	Intellectual Property
JTAG	Joint Test Action Group
LED	Light Emitting Diode
LSB	Least Significant Bit(s)
LVDS	Low Voltage Differential Signaling
LVTTL	Low Voltage Transistor Logic level
MGT	Multi-Gigabit Transceiver
MSB	Most Significant Bit(s)
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PCIe	PCI Express
PLL	Phase Locked Loop
pps	Pulse Per Second
QDR	Quadruple Data rate
SDRAM	Synchronous Dynamic Random Access memory

sFPDP	Serial FPDP
SPI	Serial Peripheral Interconnect
SRAM	Synchronous Random Access memory
SRIO	Serial Input/Output
SSC	Spread Spectrum Clocking
TTL	Transistor Logic level
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

**Table 1: Glossary**

## 1.2 Related Documents

- ANSI/VITA 46.0-2007 Rev1.2, April 2008
- ANSI/VITA 65-2010 Rev1.0, June 2010
- ANSI/VITA 48.2-2010 Rev1.0, July 2010
- ANSI/VITA 57.1-2010 Rev1.1, February 2010
- IEEE 1101.2-1992 IEEE Standard for Mechanical Core Specifications for Conduction-Cooled Eurocards

## 2 General description

The VP680 is a high performance ANSI/VITA 46.0 VPX standard compliant card with advanced digital signal processing capabilities. The design has been targeted for customer programmable implementations of complex FPGA algorithms for Digital Signal Processing (DSP) applications. The VP680 product is in the 3U VPX form factor, offering various direct on-board interface options that are closely coupled to large - fast on-board memory resources of the Xilinx Virtex™-6 FPGA. The VP680 is an excellent choice for high performance applications that require the use of accelerated frequency-domain algorithms such as with FFTs. 4DSP offers many off-the-shelf Intellectual Property (IP) cores for applications that require the highest level of performance.

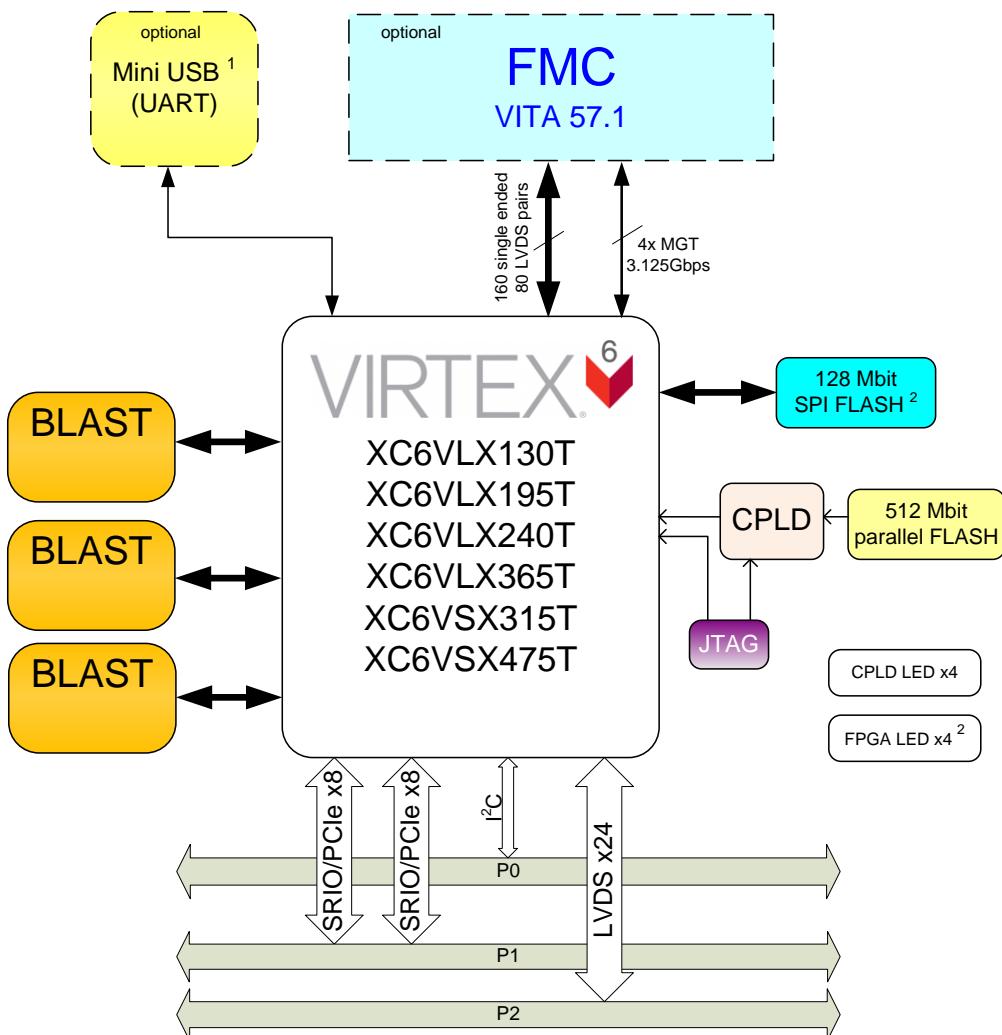


Figure 1: VP680 block diagram

<sup>1</sup> UART over USB is not available on conduction cooled VP680

<sup>2</sup> Refer to the Appendix for Errata.

## 2.1 OpenVPX

The VP680 is configurable due to the FPGA and can therefore support quite a few profiles. The reference design support x4 PCIe Gen1 and therefore matches with the following profiles:

- MOD3-PAY-1D-16.2.6-1 (only using lane 0-1)
- MOD3-PAY-2F-16.2.7-1 (only using DP01)
- MOD3-PAY-1F4U-16.2.8-1 (only using DP01)

Other profiles may be supported but requires a modification in the FPGA firmware.

## 3 Hardware Specifications

### 3.1 Phycisal specifications

The VP680 is a 3U (100x160mm) module that can be ordered as air-cooled module or conduction cooled module.

#### 3.1.1 Air-cooled

The air-cooled VP680 complies with the physical dimensions given in ANSI/VITA 46.0 with the exception that the typical PCB thickness is 2.1mm instead of 1.6mm. Normally this should not be an issue for board sliders in an air-cooled system enclosure, but in special cases 4DSP can provide a PCB thickness of 1.6mm. Please contact 4DSP.

The weight of an air cooled VP680, including front panel and BLASTs, excluding FMC is 192 grams.

#### 3.1.2 Conduction cooled

The conduction cooled VP680 is a 1.0" pitch module that complies with ANSI/VITA 48.2 with the exception that the clamshell is 4.96mm longer than specified in the VITA 48.2 standard. The clamshell thermal solution is designed to accommodate an FMC bezel which requires extra length. If this is an issue, please contact 4DSP.

The clamshell allows system integrators to use their own FMC modules and FMC bezel designs. The clamshell provides additional VPX connector protection for 2-Level Maintenance requirements. Please contact 4DSP for full 2-Level Maintenance support.

The dimensions of the conduction-cooled clamshell are depicted in the following figure.

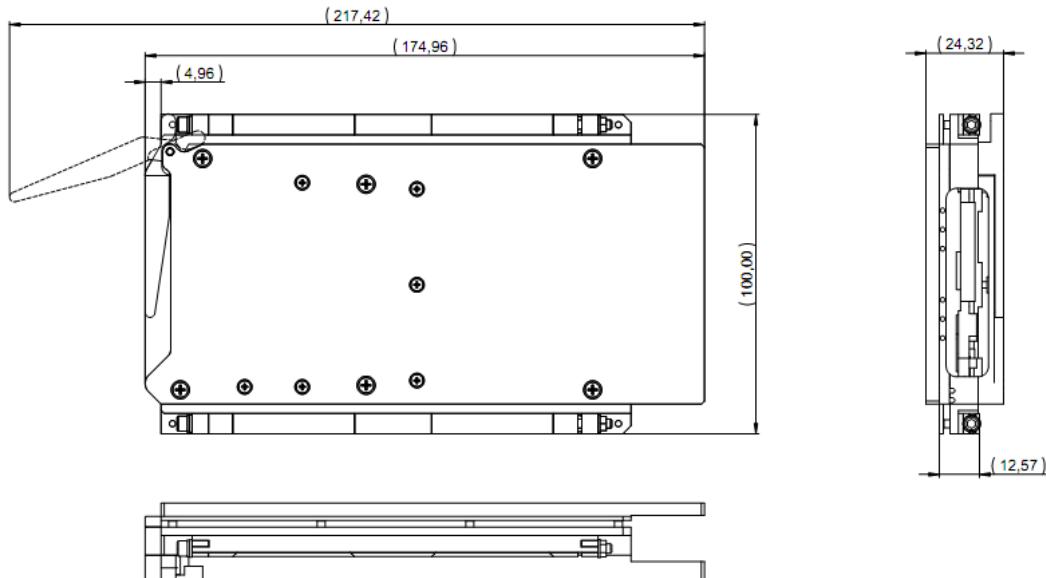


Figure 2: Conduction-cooled clamshell dimensions (mm)

### 3.1.3 Backplane keying

Both alignment keys 1 and 2 are placed by default with the un-keyed version (1-1469492-9). Contact 4DSP if specific keying is required.

### 3.1.4 Front panel layout

There are two air cooled front options; with and without FMC bezel cut-out. The front side of the conduction cooled module has an FMC bezel cut-out as well as some small holes for LED viewing.

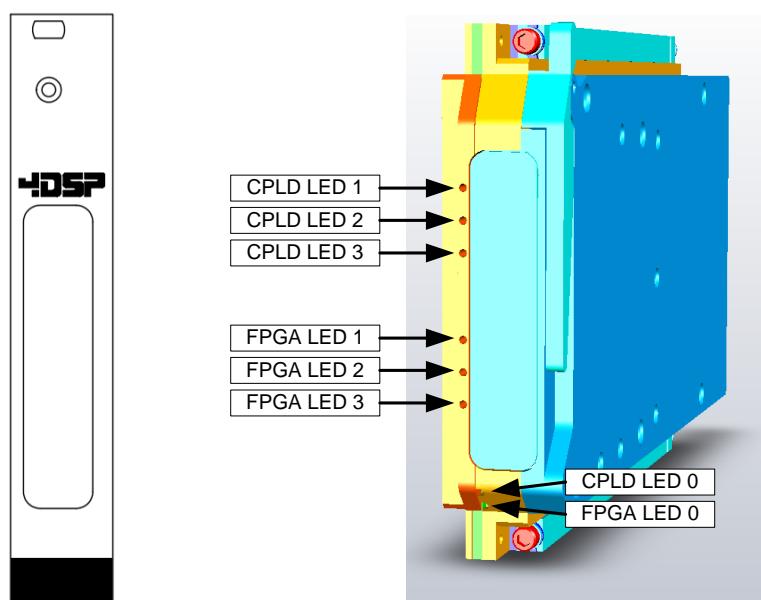


Figure 3: Air cooled front (left) and conduction cooled front (right)

### 3.2 VPX P0 Connector

P0 connector is loaded with three power wafers, three single ended wafers, and two differential wafers. The following table shows the OpenVPX definition for the P0 connector contacts.

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Vs1	Vs1	Vs1	N.C.	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	N.C.	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	N.C.	Vs3	Vs3	Vs3
4	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO
5	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1
6	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*
7	TCK	GND	TDO	TDI	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	AUX_CLK-	AUX_CLK+	GND

Table 2: VPX P0 connector pin assignment

#### 3.2.1 Power supply

Power is supplied to the VP680 on VPX P0 connector through three power supply voltages; Vs1, Vs2, and Vs3. The voltage levels are respectively 12V, 3.3V, and 5V. Several on-board DC-DC converters generate the appropriate voltage rails for the different devices and interfaces present on board. The maximum power drawn from the backplane is as follows:

- Vs1 (12V) : Max. 12 Watt
- Vs2 (3.3V) : Max. 30 Watt
- Vs3 (5V) : Max. 30 Watt

These numbers include the maximum power that can be consumed by an AV57.1 compliant FMC.

The auxiliary power supplies -12V\_Aux and +12V\_Aux are not connected. The auxiliary power supply 3.3V\_Aux is only used to pull up signals Gdiscrete1 and MaskableReset#.

#### 3.2.2 Utility plane

Table 3 shows the utility plane connections to the FPGA. The connections to REF\_CLK+/- and AUX\_CLK+/- reference clocks are described in section 3.9. Signals SM2 and SM3 are not connected.

FPGA Pin	Net Name	FPGA Bank	DIR	P0, P1		
				Connector	Pin Number	Pin Name
AG12	GA0#	33	I	P0	A6	GA0*
AL13	GA1#	33	I	P0	B6	GA1*
AK13	GA2#	33	I	P0	F6	GA2*
AH14	GA3#	33	I	P0	G6	GA3*
AH13	GA4#	33	I	P0	F5	GA4*

AN14	GAP#	33	I	P0	G5	GAP*
AP14	NVMRO	33	I	P0	A4	NVMRO
L29	I2C_SCL_VPX	15	I/O	P0	B5	SM0
R27	I2C_SDA_VPX	15	I/O	P0	A5	SM1
AC12	SYSRESET_I#	33	I	P0	B4	SYSRESET*
J24	SYSRESET_O#	24	O			
H23	GDISCRETE1_I	24	I	P1	G1	GDiscrete1
M22	GDISCRETE1_O	24	O			
AE22	MASKABLERESET#	24	I	P1	G15	MaskableReset*
G23	SYS_CON#	24	I	P1	G5	SYS_CON*

**Table 3: Utility plane connections**

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements level translation.

### 3.2.3 System reset (SYSRESET\*)

The system reset signal is implemented as input to the FPGA (SYSRESET\_I#) and as output from the FPGA and CPLD (SYSRESET\_O#). The VP680 will actively drive SYSRESET\* low until FPGA configuration is finished, after which SYSRESET\* is released (Hi-Z).

### 3.2.4 Bussed GPIO (GDiscrete1)

The general purpose I/O signal is implemented as input (GDISCRETE1\_I) and as output (GDISCRETE1\_O). When GDISCRETE1\_O is driven low, the VP680 will actively drive GDiscrete1 low. When GDISCRETE1\_O is driven high, GDiscrete1 is placed in a high impedance state.

### 3.2.5 Battery supply (P1-VBAT)

VBATT connection on the FPGA is used for data stream encryption and needs a continuous power source. The battery supply from the VPX backplane is used to provide FPGA VBATT. A maximum of 15 $\mu$ A is drawn from the VPX backplane.

## 3.3 VPX P1 Connector

The P1 connector has all positions loaded with differential wafers. A total of 32 differential pairs are available configured as 16 transceiver pairs. The VP680 connects all of those signals to MGT blocks on the FPGA. Possible applications are for instance two times 8 lanes PCI Express or other high-speed differential protocols like Aurora or sFPDP. The single ended signals are part of the utility plane described in section 3.2.2.

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	Gdiscrete1	GND	P1-TX0-	P1-TX0+	GND	P1-RX0-	P1-RX0+
2	GND	P1-TX1-	P1-TX1+	GND	P1-RX1-	P1-RX1+	GND
3	P1-VBAT	GND	P1-TX2-	P1-TX2+	GND	P1-RX2-	P1-RX2+
4	GND	P1-TX3-	P1-TX3+	GND	P1-RX3-	P1-RX3+	GND

5	SYS_CON*	GND	P1-TX4-	P1-TX4+	GND	P1-RX4-	P1-RX4+
6	GND	P1-TX5-	P1-TX5+	GND	P1-RX5-	P1-RX5+	GND
7	N.C.	GND	P1-TX6-	P1-TX6+	GND	P1-RX6-	P1-RX6+
8	GND	P1-TX7-	P1-TX7+	GND	P1-RX7-	P1-RX7+	GND
9	N.C.	GND	P1-TX8-	P1-TX8+	GND	P1-RX8-	P1-RX8+
10	GND	P1-TX9-	P1-TX9+	GND	P1-RX9-	P1-RX9+	GND
11	N.C.	GND	P1-TX10-	P1-TX10+	GND	P1-RX10-	P1-RX10+
12	GND	P1-TX11-	P1-TX11+	GND	P1-RX11-	P1-RX11+	GND
13	N.C.	GND	P1-TX12-	P1-TX12+	GND	P1-RX12-	P1-RX12+
14	GND	P1-TX13-	P1-TX13+	GND	P1-RX13-	P1-RX13+	GND
15	MaskableReset*	GND	P1-TX14-	P1-TX14+	GND	P1-RX14-	P1-RX14+
16	GND	P1-TX15-	P1-TX15+	GND	P1-RX15-	P1-RX15+	GND

Table 4: VPX P1 connector pin assignment

FPGA Pin	Net Name	MGT Block	P1	
			Pin Number	Pin Name
N4	P1_RXn00	115	B1	P1_RX0-
N3	P1_RXp00		A1	P1_RX0+
M2	P1_TXn00		E1	P1_TX0-
M1	P1_TXp00		D1	P1_TX0+
L4	P1_RXn01	115	C2	P1_RX1-
L3	P1_RXp01		B2	P1_RX1+
K2	P1_TXn01		F2	P1_TX1-
K1	P1_TXp01		E2	P1_TX1+
K6	P1_RXn02	115	B3	P1_RX2-
K5	P1_RXp02		A3	P1_RX2+
H2	P1_TXn02		E3	P1_TX2-
H1	P1_TXp02		D3	P1_TX2+
J4	P1_RXn03	115	C4	P1_RX3-
J3	P1_RXp03		B4	P1_RX3+
F2	P1_TXn03		F4	P1_TX3-
F1	P1_TXp03		E4	P1_TX3+
AA4	P1_RXn04	114	B5	P1_RX4-
AA3	P1_RXp04		A5	P1_RX4+
Y2	P1_TXn04		E5	P1_TX4-
Y1	P1_TXp04		D5	P1_TX4+
W4	P1_RXn05	114	C6	P1_RX5-

W3	P1_RXp05	114	B6	P1_RX5+
V2	P1_TXn05		F6	P1_TX5-
V1	P1_TXp05		E6	P1_TX5+
U4	P1_RXn06		B7	P1_RX6-
U3	P1_RXp06	114	A7	P1_RX6+
T2	P1_TXn06		E7	P1_TX6-
T1	P1_TXp06		D7	P1_TX6+
R4	P1_RXn07		C8	P1_RX7-
R3	P1_RXp07	113	B8	P1_RX7+
P2	P1_TXn07		F8	P1_TX7-
P1	P1_TXp07		E8	P1_TX7+
AG4	P1_RXn08		B9	P1_RX8-
AG3	P1_RXp08	113	A9	P1_RX8+
AH2	P1_TXn08		E9	P1_TX8-
AH1	P1_TXp08		D9	P1_TX8+
AF6	P1_RXn09		C10	P1_RX9-
AF5	P1_RXp09	113	B10	P1_RX9+
AF2	P1_TXn09		F10	P1_TX9-
AF1	P1_TXp09		E10	P1_TX9+
AE4	P1_RXn10	113	B11	P1_RX10-
AE3	P1_RXp10		A11	P1_RX10+
AD2	P1_TXn10		E11	P1_TX10-
AD1	P1_TXp10		D11	P1_TX10+
AC4	P1_RXn11	113	C12	P1_RX11-
AC3	P1_RXp11		B12	P1_RX11+
AB2	P1_TXn11		F12	P1_TX11-
AB1	P1_TXp11		E12	P1_TX11+
AP6	P1_RXn12	112	B13	P1_RX12-
AP5	P1_RXp12		A13	P1_RX12+
AP2	P1_TXn12		E13	P1_TX12-
AP1	P1_TXp12		D13	P1_TX12+
AM6	P1_RXn13	112	C14	P1_RX13-
AM5	P1_RXp13		B14	P1_RX13+
AN4	P1_TXn13		F14	P1_TX13-
AN3	P1_TXp13		E14	P1_TX13+
AL4	P1_RXn14	112	B15	P1_RX14-
AL3	P1_RXp14		A15	P1_RX14+
AM2	P1_TXn14		E15	P1_TX14-
AM1	P1_TXp14		D15	P1_TX14+

AJ4	P1_RXn15	112	C16	P1_RX15-
AJ3	P1_RXp15		B16	P1_RX15+
AK2	P1_TXn15		F16	P1_TX15-
AK1	P1_TXp15		E16	P1_TX15+

**Table 5: VPX P1 connections**

### 3.4 VPX P2 Connector

P2 connector has all positions loaded with differential wafers. A total of 32 differential pairs are available. The VP680 connects 24 differential pairs to LVDS capable I/O on the FPGA. The FPGA can use each differential pair as either input or output. The remaining differential pairs and the single ended signals are not connected.

	Row G	Row F	Row E	Row D	Row C	Row B	Row A
1	N.C.	GND	P2-DP1-	P2-DP1+	GND	P2-DP0-	P2-DP0+
2	GND	P2-DP3-	P2-DP3+	GND	P2-DP2-	P2-DP2+	GND
3	N.C.	GND	P2-DP5-	P2-DP5+	GND	P2-DP4-	P2-DP4+
4	GND	P2-DP7-	P2-DP7+	GND	P2-DP6-	P2-DP6+	GND
5	N.C.	GND	P2-DP9-	P2-DP9+	GND	P2-DP8-	P2-DP8+
6	GND	P2-DP11-	P2-DP11+	GND	P2-DP1-	P2-DP10+	GND
7	N.C.	GND	P2-DP13-	P2-DP13+	GND	P2-DP12-	P2-DP12+
8	GND	P2-DP15-	P2-DP15+	GND	P2-DP14-	P2-DP14+	GND
9	N.C.	GND	P2-DP17-	P2-DP17+	GND	P2-DP16-	P2-DP16+
10	GND	P2-DP19-	P2-DP19+	GND	P2-DP18-	P2-DP18+	GND
11	N.C.	GND	P2-DP21-	P2-DP21+	GND	P2-DP20-	P2-DP20+
12	GND	P2-DP23-	P2-DP23+	GND	P2-DP22-	P2-DP22+	GND
13	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
14	GND	N.C.	N.C.	GND	N.C.	N.C.	GND
15	N.C.	GND	N.C.	N.C.	GND	N.C.	N.C.
16	GND	N.C.	N.C.	GND	N.C.	N.C.	GND

**Table 6: VPX P2 connector pin assignments**

FPGA Pin	Net Name	P2	
		Pin Number	Pin Name
AP9	P2_DPN00	B1	P2_DP0-
AN9	P2_DPP00	A1	P2_DP0+
AL9	P2_DPN01	E1	P2_DP1-
AK9	P2_DPP01	D1	P2_DP1+
AL8	P2_DPN02	C2	P2_DP2-

AK8	P2_DPp02	B2	P2_DP2+
AJ9	P2_DPn03	F2	P2_DP3-
AH9	P2_DPp03	E2	P2_DP3+
AH8	P2_DPn04	B3	P2_DP4-
AG8	P2_DPp04	A3	P2_DP4+
AF10	P2_DPn05	E3	P2_DP5-
AF9	P2_DPp05	D3	P2_DP5+
AE9	P2_DPn06	C4	P2_DP6-
AD9	P2_DPp06	B4	P2_DP6+
AC9	P2_DPn07	F4	P2_DP7-
AD10	P2_DPp07	E4	P2_DP7+
AB10	P2_DPn08	B5	P2_DP8-
AC10	P2_DPp08	A5	P2_DP8+
AC24	P2_DPn09	E5	P2_DP9-
AC23	P2_DPp09	D5	P2_DP9+
AB23	P2_DPn10	C6	P2_DP10-
AA23	P2_DPp10	B6	P2_DP10+
AA24	P2_DPn11	F6	P2_DP11-
Y24	P2_DPp11	E6	P2_DP11+
V23	P2_DPn12	B7	P2_DP12-
U23	P2_DPp12	A7	P2_DP12+
T23	P2_DPn13	E7	P2_DP13-
T24	P2_DPp13	D7	P2_DP13+
N24	P2_DPn14	C8	P2_DP14-
N23	P2_DPp14	B8	P2_DP14+
L24	P2_DPn15	F8	P2_DP15-
M23	P2_DPp15	E8	P2_DP15+
M10	P2_DPn16	B9	P2_DP16-
L10	P2_DPp16	A9	P2_DP16+
K9	P2_DPn17	E9	P2_DP17-
L9	P2_DPp17	D9	P2_DP17+
F10	P2_DPn18	C10	P2_DP18-
F9	P2_DPp18	B10	P2_DP18+
E9	P2_DPn19	F10	P2_DP19-
E8	P2_DPp19	E10	P2_DP19+
D9	P2_DPn20	B11	P2_DP20-
C9	P2_DPp20	A11	P2_DP20+
D10	P2_DPn21	E11	P2_DP21-
C10	P2_DPp21	D11	P2_DP21+

C8	P2_DPn22	C12	P2_DP22-
B8	P2_DPx22	B12	P2_DP22+
A8	P2_DPn23	F12	P2_DP23-
A9	P2_DPx23	E12	P2_DP23+

**Table 7: VPX P2 connections**

### 3.5 Virtex-6 FPGA device

The Virtex-6 FPGA device is the DSP processing node of the VP680. Any Virtex-6 FPGA device from the Virtex-6 SXT and LXT family in an 1156 balls fine line ball grid array package can be ordered:

- XC6VLX130T
- XC6VLX195T
- XC6VLX240T
- XC6VLX365T
- XC6VSX315T
- XC6VSX475T

### 3.6 Front panel I/O

The VP680 reserves the front panel I/O area for the FMC site. On the air-cooled VP680 there is a UART over USB option for debugging purposes. In addition there are some status and debug LEDs available.

#### 3.6.1 UART over USB

One UART connection is optionally available on the front panel via a mini USB connector (location depicted in Figure 7). The serial interface is made using a USB to UART Bridge (CP2102). The UART side connects to the FPGA.

FPGA Pin	Net Name	FPGA Bank	DIR	CP2102	
				Pin Number	Pin Name
D11	UART_TXD	35	O	25	RXD
H15	UART_RXD	36	I	26	TXD

**Table 8: UART connections**

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements level translation.

#### 3.6.2 Status LEDs (CPLD)

Four LEDs are connected to the CPLD for board status purposes. There is a pre-defined function for these LEDs. One LED (CPLD LED 0) is located on the component side of the VP680. The other LEDs are located on the solder side of the VP680 (see Figure 3).

	OFF	ON	FLASHING
<b>LED 0 (red)</b>	Power OK	Power not OK (ex. VADJ)	VADJ not OK
<b>LED 1 (red)</b>	FPGA configured	FPGA not configured	Loading to FLASH
<b>LED 2 (red)</b>	FLASH idle	FLASH busy	Safety configuration loaded into FPGA, or attempted to load.
<b>LED 3 (red)</b>	FPGA expects 100 MHz on VPX REF_CLK+/-.	FPGA expects 25 MHz on VPX REF_CLK+/-.	CRC error during FPGA configuration.

Table 9: CPLD LED board status

### 3.6.3 Debug LEDs (FPGA)

Four red LEDs are connected to the FPGA for debugging purposes. There is no pre-defined function for these LEDs. One LED (FPGA\_LED0) is located on the component side of the VP680. The other LEDs are located on the solder side of the VP680 (see Figure 3).

To turn on a LED drive the signal low. To turn a LED off, make the signal Hi-Z.

FPGA Pin	Net Name	FPGA Bank	DIR
F31	FPGA_LED0	16	O
G32	FPGA_LED1	16	O
L26	FPGA_LED2	16	O
L25	FPGA_LED3	16	O

Table 10: LED connections

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements proper level translation.

## 3.7 FPGA Mezzanine Card (FMC)

The FPGA interfaces to an FPGA Mezzanine Card (FMC) via a high pin count (HPC) VITA 57.1 site. All banks (LA, HA, HB) are connected to the FPGA. The FMC site provides flexibility for adding analog and/or digital I/O via customer developed, third party or 4DSP FMC boards. 4DSP offers a wide variety of FMC cards that can be used on the VP680. Among others:

- FMC103: 4-ch A/D 210 Msps @ 12-bits
- FMC104: 4-ch A/D 250 Msps @ 14-bits
- FMC107: 8-ch A/D 65 Msps @ 12-bits
- FMC108: 8-ch A/D 250 Msps @ 14-bits
- FMC204: 4-ch DA 1 Gsps @ 16-bits
- FMC150: Dual A/D. Dual D/A Channel
  - 2-ch A/D 250 Msps @ 14-bits
  - 2-ch D/A 800 Msps @ 16-bits

- FMC110: Dual A/D. Dual D/A Channel
  - 2-ch A/D 1 Gsps @ 12-bits
  - 2-ch D/A 1 Gsps @ 16-bits
- FMC122: Single-Dual Channel A/D
  - 1-ch A/D 2.50 Gsps @ 8-bits, or
  - 2-ch A/D 1.25 Gsps @ 8-bits
- FMC125: Quad-Dual-Single Channel A/D
  - 1-ch A/D 5.00 Gsps @ 8-bits, or
  - 2-ch A/D 2.50 Gsps @ 8-bits, or
  - 4-ch A/D 1.25 Gsps @ 8-bits
- FMC126: Quad-Dual-Single Channel A/D
  - 1-ch A/D 5.00 Gsps @ 10-bits, or
  - 2-ch A/D 2.50 Gsps @ 10-bits, or
  - 4-ch A/D 1.25 Gsps @ 10-bits

### 3.7.1 Bank A (LA, HA) connections

Differential routing is applied with matched delay on all pair within bank A (LA, HA).

FPGA Pin	Net Name	FMC HPC	
		Pin Number	Pin Name
AF33	LA_N0_CC	G7	LA00_N_CC
AE33	LA_P0_CC	G6	LA00_P_CC
AC30	LA_N1_CC	D9	LA01_N_CC
AD30	LA_P1_CC	D8	LA01_P_CC
AC29	LA_N2	H8	LA02_N
AD29	LA_P2	H7	LA02_P
AF34	LA_N3	G10	LA03_N
AE34	LA_P3	G9	LA03_P
AC28	LA_N4	H11	LA04_N
AB28	LA_P4	H10	LA04_P
AE32	LA_N5	D12	LA05_N
AD32	LA_P5	D11	LA05_P
AC27	LA_N6	C11	LA06_N
AB27	LA_P6	C10	LA06_P
AG32	LA_N7	H14	LA07_N
AG33	LA_P7	H13	LA07_P
AB26	LA_N8	G13	LA08_N
AA26	LA_P8	G12	LA08_P
AF31	LA_N9	D15	LA09_N

AG31	LA_P9	D14	LA09_P
AC25	LA_N10	C15	LA10_N
AB25	LA_P10	C14	LA10_P
AB33	LA_N11	H17	LA11_N
AC33	LA_P11	H16	LA11_P
AD31	LA_N12	G16	LA12_N
AE31	LA_P12	G15	LA12_P
Y26	LA_N13	D18	LA13_N
AA25	LA_P13	D17	LA13_P
V29	LA_N14	C19	LA14_N
U28	LA_P14	C18	LA14_P
U30	LA_N15	H20	LA15_N
U31	LA_P15	H19	LA15_P
T25	LA_N16	G19	LA16_N
U25	LA_P16	G18	LA16_P
W34	LA_N17_CC	D21	LA17_N_CC
V34	LA_P17_CC	D20	LA17_P_CC
W30	LA_N18_CC	C23	LA18_N_CC
V30	LA_P18_CC	C22	LA18_P_CC
V27	LA_N19	H23	LA19_N
V28	LA_P19	H22	LA19_P
V33	LA_N20	G22	LA20_N
V32	LA_P20	G21	LA20_P
Y31	LA_N21	H26	LA21_N
Y32	LA_P21	H25	LA21_P
Y34	LA_N22	G25	LA22_N
Y33	LA_P22	G24	LA22_P
Y29	LA_N23	D24	LA23_N
W29	LA_P23	D23	LA23_P
W32	LA_N24	H29	LA24_N
W31	LA_P24	H28	LA24_P
Y27	LA_N25	G28	LA25_N
Y28	LA_P25	G27	LA25_P
V25	LA_N26	D27	LA26_N
W25	LA_P26	D26	LA26_P
W26	LA_N27	C27	LA27_N
W27	LA_P27	C26	LA27_P
T29	LA_N28	H32	LA28_N
T28	LA_P28	H31	LA28_P

R34	LA_N29	G31	LA29_N
R33	LA_P29	G30	LA29_P
T31	LA_N30	H35	LA30_N
T30	LA_P30	H34	LA30_P
T34	LA_N31	G34	LA31_N
T33	LA_P31	G33	LA31_P
U27	LA_N32	H38	LA32_N
U26	LA_P32	H37	LA32_P
U32	LA_N33	G37	LA33_N
U33	LA_P33	G36	LA33_P

**Table 11: FMC LA connections**

FPGA Pin	Net Name	FMC HPC	
		Pin Number	Pin Name
AG30	HA_N0_CC	F5	HA00_N_CC
AF30	HA_P0_CC	F4	HA00_P_CC
AE26	HA_N1_CC	E3	HA01_N_CC
AF26	HA_P1_CC	E2	HA01_P_CC
AD26	HA_N2	K8	HA02_N
AD25	HA_P2	K7	HA02_P
AJ32	HA_N3	J7	HA03_N
AJ31	HA_P3	J6	HA03_P
AJ30	HA_N4	F8	HA04_N
AJ29	HA_P4	F7	HA04_P
AK32	HA_N5	E7	HA05_N
AK33	HA_P5	E6	HA05_P
AK31	HA_N6	K11	HA06_N
AL31	HA_P6	K10	HA06_P
AL33	HA_N7	J10	HA07_N
AM33	HA_P7	J9	HA07_P
AM32	HA_N8	F11	HA08_N
AN32	HA_P8	F10	HA08_P
AP33	HA_N9	E10	HA09_N
AP32	HA_P9	E9	HA09_P
AM31	HA_N10	K14	HA10_N
AL30	HA_P10	K13	HA10_P
AD27	HA_N11	J13	HA11_N
AE27	HA_P11	J12	HA11_P

AH32	HA_N12	F14	HA12_N
AH33	HA_P12	F13	HA12_P
AE29	HA_N13	E13	HA13_N
AE28	HA_P13	E12	HA13_P
AH34	HA_N14	J16	HA14_N
AJ34	HA_P14	J15	HA14_P
AF29	HA_N15	F17	HA15_N
AF28	HA_P15	F16	HA15_P
AK34	HA_N16	E16	HA16_N
AL34	HA_P16	E15	HA16_P
AG28	HA_N17_CC	K17	HA17_N_CC
AG27	HA_P17_CC	K16	HA17_P_CC
AN34	HA_N18_CC	J19	HA18_N
AN33	HA_P18_CC	J18	HA18_P
AH30	HA_N19	F20	HA19_N
AH29	HA_P19	F19	HA19_P
AA33	HA_N20	E19	HA20_N
AA34	HA_P20	E18	HA20_P
AA31	HA_N21	K20	HA21_N
AA30	HA_P21	K19	HA21_P
AC34	HA_N22	J22	HA22_N
AD34	HA_P22	J21	HA22_P
AB31	HA_N23	K23	HA23_N
AB30	HA_P23	K22	HA23_P

Table 12: FMC HA connections

### 3.7.2 Bank B (HB) connections

Differential routing is applied with matched delay on all pair within bank B (HB).

FPGA Pin	Net Name	FMC HPC	
		Pin Number	Pin Name
AJ27	HB_N0_CC	K26	HB00_N_CC
AK27	HB_P0_CC	K25	HB00_P_CC
AH28	HB_N1	J25	HB01_N
AH27	HB_P1	J24	HB01_P
AM30	HB_N2	F23	HB02_N
AN30	HB_P2	F22	HB02_P
AG26	HB_N3	E22	HB03_N

AG25	HB_P3	E21	HB03_P
AP31	HB_N4	F26	HB04_N
AP30	HB_P4	F25	HB04_P
AK29	HB_N5	E25	HB05_N
AL29	HB_P5	E24	HB05_P
AH24	HB_N6_CC	K29	HB06_N_CC
AH23	HB_P6_CC	K28	HB06_P_CC
AP29	HB_N7	J28	HB07_N
AN29	HB_P7	J27	HB07_P
AK28	HB_N8	F29	HB08_N
AL28	HB_P8	F28	HB08_P
AM28	HB_N9	E28	HB09_N
AN28	HB_P9	E27	HB09_P
AJ25	HB_N10	K32	HB10_N
AH25	HB_P10	K31	HB10_P
AP24	HB_N11	J31	HB11_N
AP25	HB_P11	J30	HB11_P
AM26	HB_N12	F32	HB12_N
AL26	HB_P12	F31	HB12_P
AK24	HB_N13	E31	HB13_N
AJ24	HB_P13	E30	HB13_P
AP26	HB_N14	K35	HB14_N
AP27	HB_P14	K34	HB14_P
AL25	HB_N15	J34	HB15_N
AM25	HB_P15	J33	HB15_P
AN24	HB_N16	F35	HB16_N
AN25	HB_P16	F34	HB16_P
AM27	HB_N17_CC	K38	HB17_N_CC
AN27	HB_P17_CC	K37	HB17_P_CC
AL24	HB_N18	J37	HB18_N
AK23	HB_P18	J36	HB18_P
AJ26	HB_N19	E34	HB19_N
AK26	HB_P19	E33	HB19_P
AA29	HB_N20	F38	HB20_N
AA28	HB_P20	F37	HB20_P
AC32	HB_N21	E37	HB21_N
AB32	HB_P21	E36	HB21_P

**Table 13: FMC HB connections**

### 3.7.3 Gigabit transceiver connections

The VP680 connects the lowest four gigabit transceivers to MGT blocks on the FPGA, the other transceivers are left unconnected. The reference clocks are described in section 3.9.4.

FPGA Pin	Net Name	MGT Block	FMC HPC	
			Pin Number	Pin Name
D2	DP_C2M_n0	116	C3	DP0_C2M_N
D1	DP_C2M_p0		C2	DP0_C2M_P
G4	DP_M2C_n0		C7	DP0_M2C_N
G3	DP_M2C_p0		C6	DP0_M2C_P
C4	DP_C2M_n1	116	A23	DP1_C2M_N
C3	DP_C2M_p1		A22	DP1_C2M_P
E4	DP_M2C_n1		A3	DP1_M2C_N
E3	DP_M2C_p1		A2	DP1_M2C_P
B2	DP_C2M_n2	116	A27	DP2_C2M_N
B1	DP_C2M_p2		A26	DP2_C2M_P
D6	DP_M2C_n2		A7	DP2_M2C_N
D5	DP_M2C_p2		A6	DP2_M2C_P
A4	DP_C2M_n3	116	A31	DP3_C2M_N
A3	DP_C2M_p3		A30	DP3_C2M_P
B6	DP_M2C_n3		A11	DP3_M2C_N
B5	DP_M2C_p3		A10	DP3_M2C_P

Table 14: FMC MGT connections

### 3.7.4 Miscellaneous FMC connections

The differential clock connections are described in section 3.9.1. The global address pins (GA0 and GA1) on the FMC site are tied to ground. PG\_C2M is driven by glue logic in the CPLD which monitors the voltages VADJ, 3P3V, and 12P0V applied to the FMC. Power pin 3P3VAUX is connected to 3P3V on the VP680.

FPGA Pin	Net Name	FPGA Bank	DIR	FMC HPC	
				Pin Number	Pin Name
F23	I2C_SCL_FMC	24	IO	C30	SCL
F24	I2C_SDA_FMC	24	IO	C31	SDA
D15	PG_M2C	36	I	F1	PG_M2C
C15	PRSNT_M2C_L	36	I	H2	PRSNT_M2C_L

Table 15: Miscellaneous FMC connections

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements proper level translation.

### 3.7.1 I/O Standard Support

The VP680 is optimized for differential signalling, but any single ended I/O standard supported by the FPGA can be used as well. FMC bank A (LA, HA) connects to FPGA banks powered by VADJ. FMC bank B connects an FPGA bank powered by VIO\_B\_M2C, except:

- HB\_20p/n, which connect to a VADJ powered FPGA bank
- HB\_21p/n, which connect to a VADJ powered FPGA bank

Reference voltages from the FMC (VREF\_A\_M2C, VREF\_B\_M2C) are not connected. I/O standards that require a reference voltage should use the internal Vref features of the FPGA. The following reference voltages are supported:

- 0.6V
- 0.75V
- 0.90V
- 1.1V
- 1.25V

For I/O standards that require Digitally Controlled Impedance (DCI) please contact 4DSP.

### 3.7.2 VADJ Programming

After power up VADJ is in power down state until the FPGA is configured. After FPGA configuration VADJ is set to one of the voltage from Table 16. Glue logic is implemented by two signals driven by the FPGA; FP\_CP\_0 and FP\_CP\_1 (see also Table 30). Please contact 4DSP for 1.25V and 0.8V VADJ voltage options.

FP_CP_0	FP_CP_1	VADJ
0	0	2.5V (default)
1	0	1.8V
0	1	1.5V
1	1	1.2V

Table 16: VADJ voltage options

## 3.8 BLAST sites

Thanks to the availability of three BLAST sites a wide variety of memory and processing modules can be connected to the FPGA. For each BLAST site it is possible to choose from the list of available BLAST modules.

For more information about the available BLASTs on the VP680 please consult the following page: BLAST modules <http://www.4dsp.com/BLAST.htm>

Due to its small form factor and ease of design, the BLAST modules enable a rapid solution for custom memory or processing requirements.

BLAST Form Factor	BLAST 0	BLAST 1	BLAST 2
Single BLAST	YES	YES	YES
Single Extended BLAST	YES	YES	YES
Double BLAST	Contact 4DSP		NO
Double Extended BLAST	Contact 4DSP		NO

**Table 17: BLAST Configuration options**

BLAST Type	BLAST 0	BLAST 1	BLAST 2
DDR3	YES	YES	YES
DDR2	YES	YES	YES
QDR	YES	YES	YES
ADV212 JPEG2000	YES	YES	YES
32GB NAND FLASH	YES	YES	YES

**Table 18: BLAST Memory/Processing options**

Power is applied depending on the BLAST type. Each BLAST site has three voltage rails:

- Vcore : 3.3V, 2.5V, 1.8V, 1.5V
- Vio : 2.5V, 1.8V, 1.5V
- Vref : 0.9V

BLAST1 does not have a separate Vio plane, but uses BLAST0 Vio.

### 3.9 Clock Tree

The VP680 clock architecture offers an efficient distribution of low jitter clocks to facilitate efficient implementation of fast off chip communication with other peripherals. The VPX backplane offers two reference clock signals (AUX\_CLK and REF\_CLK) that can be used by plug-in modules for synchronisation between different plug-in modules in a VPX system.

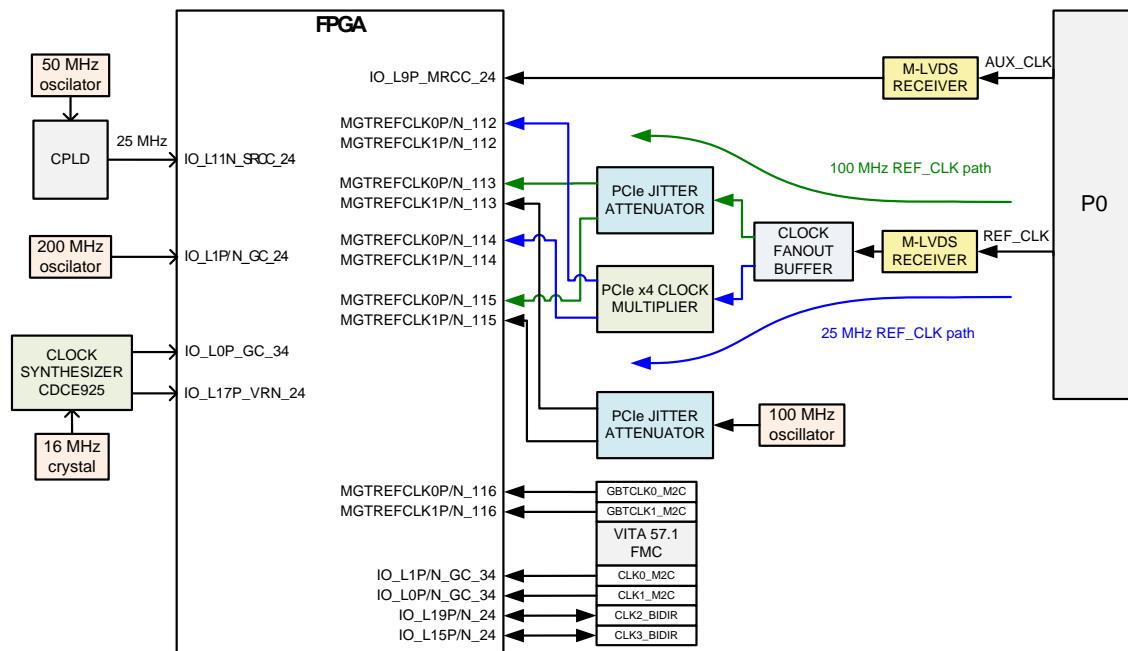


Figure 4: Clock architecture

### 3.9.1 AUX\_CLK+/- Reference Clock

AUX\_CLK is a 1pps timing reference, which is defined with relatively tight accuracy and stability specifications and is driven differentially on the backplane. This signal is typically used in OpenVPX applications to provide a high-precision hardware timing delimiter for time-based processing tasks. The VP680 buffers and translates into a single ended signal before connecting to the FPGA.

FPGA Pin	Net Name	FPGA Bank	DIR	P0		
				Connector	Pin Number	Pin Name
J25	AUX_CLK	24	I	P0	C8	AUX_CLK-
				P0	B8	AUX_CLK+

Table 19: AUX\_CLK connection

### 3.9.2 REF\_CLK+/- Reference Clock

REF\_CLK is a reference clock with tight accuracy and stability specifications and is driven differentially on the backplane. One of the uses of this signal is for all plug-in modules to synchronize to a common clock to enable the implementation of Spread Spectrum Clocking (SSC) to reduce EMI in a system (PCI Express for example defines the use of this mechanism for SSC). It is anticipated that a plug-in module will receive the reference clock and phase lock it up to the desired operational frequency.

Initial revisions of the OpenVPX specifications recommend a 25 MHz clock for this signal, but recently a suggestion was made by the OpenVPX work group to implement a 100 MHz clock which can be used directly as reference for PCI Express Generation 2 applications.

The VP680 implements a clock architecture that works for both cases, see Figure 4. Either the 25MHz clock path or the 100MHz clock path should be used. Each clock path has two

100MHz reference clocks connected to the FPGA in such a way that all MGT block can be reached.

FPGA Pin	Net name	MGT REFCLK	MGTs reached
AD5	VPX_100M_REFCLK0n	MGTREFCLK0_113	112, 113, 114
AD6	VPX_100M_REFCLK0p		
P5	VPX_100M_REFCLK1n	MGTREFCLK0_115	114, 115, 116
P6	VPX_100M_REFCLK1p		
AK5	VPX_25M_REFCLK0n	MGTREFCLK0_112	112, 113
AK6	VPX_25M_REFCLK0p		
V5	VPX_25M_REFCLK1n	MGTREFCLK0_114	113, 114, 115
V6	VPX_25M_REFCLK1p		

**Table 20: REF\_CLK connections**

Only one clock path is enabled, the other clock path is power down. Glue logic to control the clock path is implemented in the CPLD. The FPGA controls clock path selection through signal FP\_CP\_7 (see also Table 30).

FP_CP_7	Clock path selection
0	Clock path for 25MHz REF_CLK is selected
1	Clock path for 100MHz REF_CLK is selected

**Table 21: Clock path selection**

### 3.9.3 On-board MGT Reference Clock

A 100 MHz clock from an on-board low jitter oscillator is distributed to the FPGA using a jitter attenuator. This clock can be used as the reference clock for the MGT blocks. The reference clocks are connected in such a way that all MGTs can use these reference clocks.

FPGA Pin	Net name	MGT REFCLK	MGTs reached
AB5	LOCAL_REFCLK0n	MGTREFCLK1_113	112, 113, 114
AB6	LOCAL_REFCLK0p		
M5	LOCAL_REFCLK1n	MGTREFCLK1_115	114, 115, 116
M6	LOCAL_REFCLK1p		

**Table 22: On-board MGT reference clock connections**

### 3.9.4 FMC MGT Reference Clock

The FMC standard defines two high precision reference clocks that are driven from the FMC to the carrier. The VP680 connects these clocks directly to MGT reference clock inputs. The following table shows which MGTs can use these reference clocks.

FPGA Pin	Net name	MGT REFCLK	MGTs reached
H5	GBTCLK0_M2C_n	MGTREFCLK0_116	115, 116
H6	GBTCLK0_M2C_p		
F5	GBTCLK1_M2C_n	MGTREFCLK1_116	115, 116
F6	GBTCLK1_M2C_p		

**Table 23: FMC MGT reference clock connections**

### 3.9.1 FMC Clock connections

The FMC clocks are connected to LVDS capable I/O on the FPGA. CLK0 and CLK1 are connected to global clock inputs. CLK2 and CLK3 are connected to regular I/O.

FPGA Pin	Net Name	FMC HPC	
		Pin Number	Pin Name
B10	CLK0_M2C_n	H5	CLK0_M2C_N
A10	CLK0_M2C_p	H4	CLK0_M2C_P
H9	CLK1_M2C_n	G3	CLK1_M2C_N
J9	CLK1_M2C_p	G2	CLK1_M2C_P
AD22	CLK2_BIDIR_n	K5	CLK2_BIDIR_N
AC22	CLK2_BIDIR_p	K4	CLK2_BIDIR_P
AG23	CLK3_BIDIR_n	J3	CLK3_BIDIR_N
AF23	CLK3_BIDIR_p	J2	CLK3_BIDIR_P

**Table 24: FMC clock connections**

### 3.9.2 Miscellaneous clock connections

A low jitter programmable clock device (CDCE925, section 3.10.1) able to generate frequencies from 62.5MHz to 255.5MHz in steps of 0.5MHz is available. Two outputs are connected to the FPGA. Further there is a fixed 200 MHz differential clock.

FPGA Pin	Net Name	FPGA Bank	DIR	CDCE925, ECS-LVDS25		
				Device	Pin Number	Pin Name
L23	CLK_SYNTH_0	24	I	CDCE925	13	Y1
AE23	CLK_SYNTH_1	24	I	CDCE925	7	Y4
K23	CLK200_N	24	I	ECS-LVDS25	5	C-Output
K24	CLK200_P			ECS-LVDS25	4	Output

**Table 25: Miscellaneous clock connections**

## 3.10 Local I<sup>2</sup>C bus

A local I<sup>2</sup>C bus connects to three on-board slave peripherals. The FPGA should implement I<sup>2</sup>C master logic to use these peripherals. One of the peripherals is a programmable clock

device (CDCE925) which is also described in section 3.9.2. The other two peripherals are monitoring devices (ADT7411) used to measure the power on the different voltage rails as well as the temperature.

The monitoring devices can be configured in such a way that an interrupt output (MON\_INT#) is asserted when one of the parameters is out of range.

FPGA Pin	Net Name	FPGA Bank	DIR	CDCE925, ADT7411		
				Device	Pin Number	Pin Name
J32	I2C_SCL_LOCAL	16	IO	CDCE925	14	S2/SCL
				ADT7411 #1	13	SCL/SCLK
				ADT7411 #2	13	SCL/SCLK
J31	I2C_SDA_LOCAL	16	IO	CDCE925	15	S1/SDA
				ADT7411 #1	12	SDA/DIN
				ADT7411 #2	12	SDA/DIN
E11	MON_INT#	35	I	ADT7411 #1	10	INT/INT*
				ADT7411 #2	10	INT/INT*

**Table 26: Local I<sup>2</sup>C bus connections**

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements proper level translation.

### 3.10.1 Clock Synthesizer (CDCE925)

The CDCE925 is a low jitter programmable clock device able to generate frequencies from 62.5MHz to 255.5MHz in steps of 0.5MHz. This clock management approach ensures maximum flexibility to efficiently implement multi-clock domains algorithms and use memory devices at different frequencies. The clock connections to the FPGA are described in section 3.9.2. Refer to the datasheet of the CDCE925 for detailed information.

### 3.10.2 On-board Voltage and Temperature Monitoring (ADT7411)

Refer to the datasheet of the ADT7411 for detailed information. The I<sup>2</sup>C slave address is set to b'1001000' for the first device and to b'1001010' for the second device.

Parameter	Connection	Formula
On-chip temperature	ADT7411 Die Temperature	
On-chip AIN0 ( $V_{DD}$ )	+3.3V	
External temperature	FPGA Die Temperature	
External AIN3	12V	$AIN3 * 5.7$
External AIN4	1V0	$AIN4$
External AIN5	BLAST2 Vio	$AIN5 * 2.0$
External AIN6	BLAST0 Vio	$AIN6 * 2.0$
External AIN7	MGTAVTT	$AIN7$
External AIN8	MGTAVCC	$AIN8$

**Table 27: Monitoring device #1 connections**

Parameter	Connection	Formula
On-chip temperature	ADT7411 Die Temperature	
On-chip AIN0 ( $V_{DD}$ )	+3.3V	
External AIN1	BLAST0 Vcore	$AIN1 * 2$
External AIN2	BLAST1 Vcore	$AIN2 * 2$
External AIN3	5V	$AIN3 * 14.7 / 4.7$
External AIN4	0V9	$AIN4$
External AIN5	VADJ	$AIN5 * 2$
External AIN6	1V8	$AIN6$
External AIN7	BLAST2 Vcore	$AIN7 * 2$
External AIN8	2V5	$AIN8 * 2$

**Table 28: Monitoring device #2 connections**

### 3.11 Serial FLASH

A 128 Mbits serial FLASH device (S25FL128P) is available to the FPGA. This FLASH allows the storage of vital data like processor boot code and settings into a non-volatile memory.

The FLASH is operated using a standard SPI interface that can run up to 104 MHz, allowing for a page programming speed up to 208 KB/s. Reading data from the FLASH can be done at speeds up to 13 MB/s.

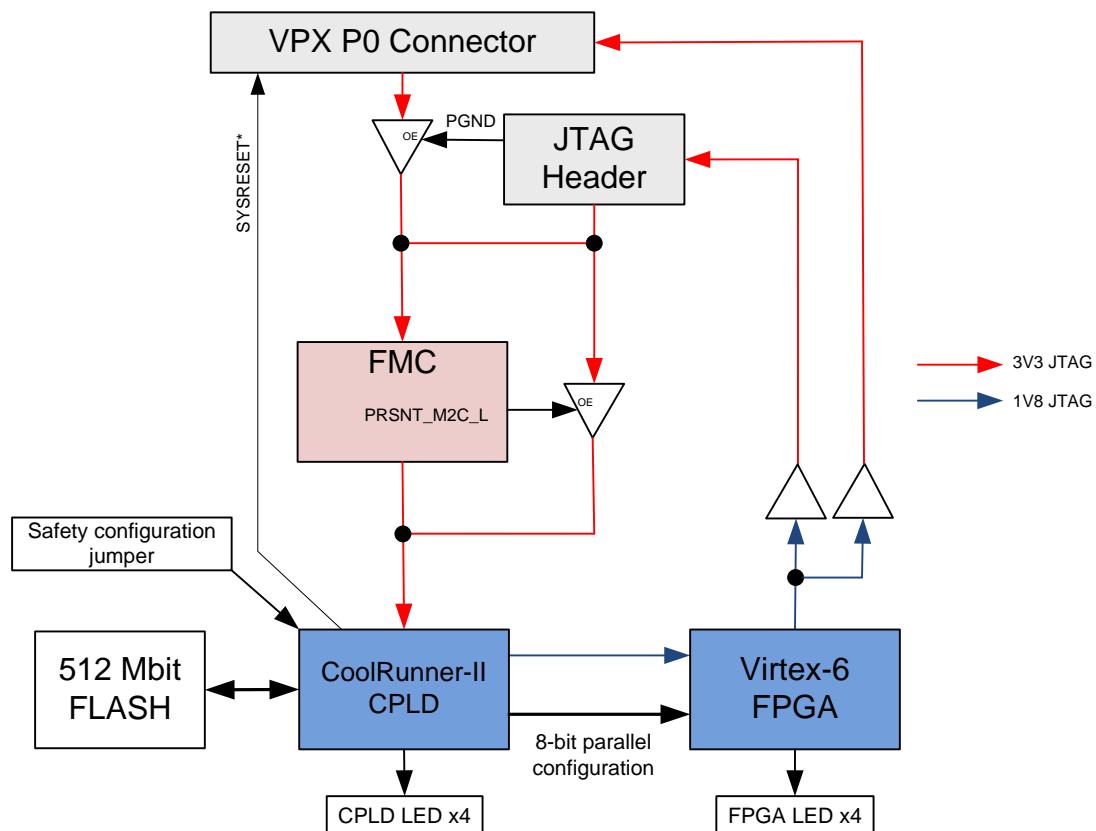
FPGA Pin	Net Name	FPGA Bank	DIR	S25FL128P	
				Pin Number	Pin Name
K13	SF_SCK	35	O	16	SCK
M13	SF_SI	35	O	15	SI
L16	SF_SO	36	I	8	SO/PO7

**Table 29: SPI FLASH connections**

The I/O standard to be assigned depends on BLAST configuration. Refer to Table 32: BLAST VIO Matrix in the Appendix. The VP680 implements proper level translation.

## FPGA Configuration

Figure 5 shows the configuration architecture on the VP680. The architecture allows FPGA configuration through the JTAG chain as well as parallel configuration from FLASH memory. The FPGA can be automatically loaded from FLASH after the VP680 powered up.



**Figure 5: Configuration architecture**

### 3.11.1 JTAG chain

The JTAG chain on the VP680 is available for configuration and debugging purposes. The JTAG chain is accessible from the VPX backplane and an on-board header (for a Xilinx

Platform USB-II cable, see Figure 7). The JTAG chain dynamically changes in the following situations:

1. Source selection
  - a. When no Xilinx Platform USB-II cable is connected to the JTAG header the pseudo ground signal (PGND) is pulled high by a resistor on the VP680 and the JTAG signals from the VPX backplane are connected to the local JTAG chain.
  - b. When a Xilinx Platform USB-II cable is connected to the JTAG header the pseudo ground signal (PGND) is pulled low by the cable and the JTAG signals from the VPX backplane are disconnected from the local JTAG chain.
2. FMC included
  - a. When no FMC card is present the PRSNT\_M2C\_L signal is pulled high by a resistor on the VP680 and the FMC's TDO is connected to the FMC's TDI. The JTAG chain is as follows: **CPLD → FPGA**.
  - b. When an FMC card is present the PRSNT\_M2C\_L signal is pulled low by the FMC card and the FMC's TDO is disconnected from the FMC's TDI. The JTAG chain is as follows: **FMC → CPLD → FPGA**.

### 3.11.2 FLASH storage

Firmware images are stored on-board in a 512Mbit FLASH device and loaded to the FPGA after power-up. By default there is space reserved for two FPGA images; a safety image and a user image. In addition the FLASH keeps board specific information like serial number, FPGA type, and BLAST information.



Figure 6: FLASH arrangement

### 3.11.3 Configuration Controller (CPLD)

As shown in Figure 5, a CoolRunner-II CPLD is present to interface between the FLASH device and the FPGA device. The CPLD implements glue logic to program and read the FLASH memory.

After power-up the configuration controller loads the user image to the FPGA. If FPGA configuration fails (for example when no user image exist or when the user image is faulty) the configuration controller continues with loading the safety image. FPGA configuration is performed in SelectMap mode.

The bus between FPGA and CPLD consist of 9 dual purpose signals. During FPGA configuration (Function 1) the bus is transferring 8-bit configuration data from CPLD to FPGA. After FPGA configuration (Function 2) the signals are used for communication between FPGA and CPLD.

FPGA Pin	Net Name	FPGA Bank	DIR	XC2C256-FT256		
				Pin Number	Function 1	Function 2
AF24	FP_CP_0	24	O	C13	D0	See section 3.7.2
AF25	FP_CP_1	24	O	A15	D1	
W24	FP_CP_2	24	O	C12	D2	COMMAND
V24	FP_CP_3	24	O	B12	D3	COMMAND
H24	FP_CP_4	24	O	D13	D4	COMMAND
H25	FP_CP_5	24	O	A14	D5	COMMAND
P24	FP_CP_6	24	I	E13	D6	DATA
R24	FP_CP_7	24	O	A13	D7	See section 3.9.2
AE24	FP_CP_8	24	I	C11	-	

Table 30: CPLD connections

### 3.11.4 User image programming

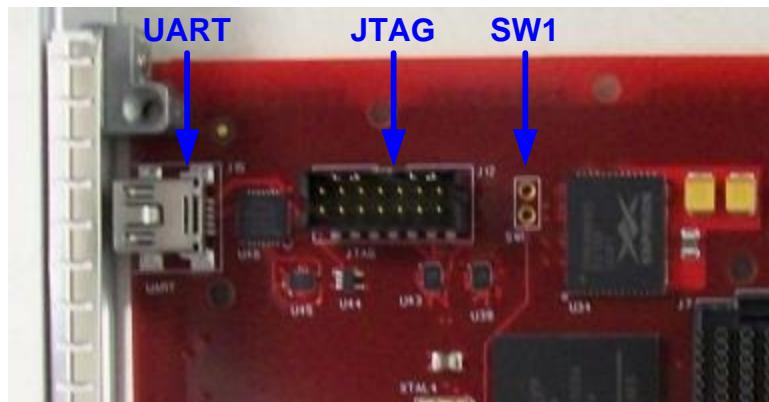
Programming the user image in FLASH should be done from a system host through the PCI Express interface using 4DSP's VP680 reference firmware design and 4FM GUI Control Application. The firmware reference design is stored in the safety image space. In factory the firmware reference design will also be programmed in the user image space.

The user image may be overwritten with an image that does not implement the FLASH update features from 4DSP's VP680 firmware reference design. In that case there are two ways to recover:

- 1) Configure the FPGA with 4DSP's VP680 firmware reference design through the JTAG chain. Then use the 4FM GUI Control Application to program a new user image in FLASH.
- 2) Power down the board, place the safety configuration jumper (section 3.11.5) and power-up. Then use the 4FM GUI Control Application to program a new user image in FLASH

### 3.11.5 Safety Configuration Jumper

A press fit jumper footprint (SW1) is located next to the JTAG programming connector. If the jumper is closed the FPGA safety image is loaded from FLASH after power-up.



**Figure 7: Connector / Jumper locations**

## 4 Environment Specifications

## 4.1 Temperature

## Operating temperature

- 0°C to +70°C (Commercial)
- -40°C to +85°C (Industrial)

Storage temperature:

- -40°C to +120°C

## 4.2 Convection cooling

The air flow provided by the chassis fans the VP680 is enclosed in will dissipate the heat generated by the on board components. A minimum airflow of 300 LFM is recommended.

4DSP's warranty does not cover boards on which the maximum allowed temperature has been exceeded.

### 4.3 Conduction cooling

The VP680 is designed for conduction cooling according to ANSI/VITA 48.2. The module has primary side retainers. Slot pitch is 1.00 inch.

## 5 Safety

This module presents no hazard to the user.

## 6 EMC

This module is designed to operate from within an enclosed host system, which is built to provide EMC shielding. Operation within the EU EMC guidelines is not guaranteed unless it is installed within an adequate host system. This module is protected from damage by fast

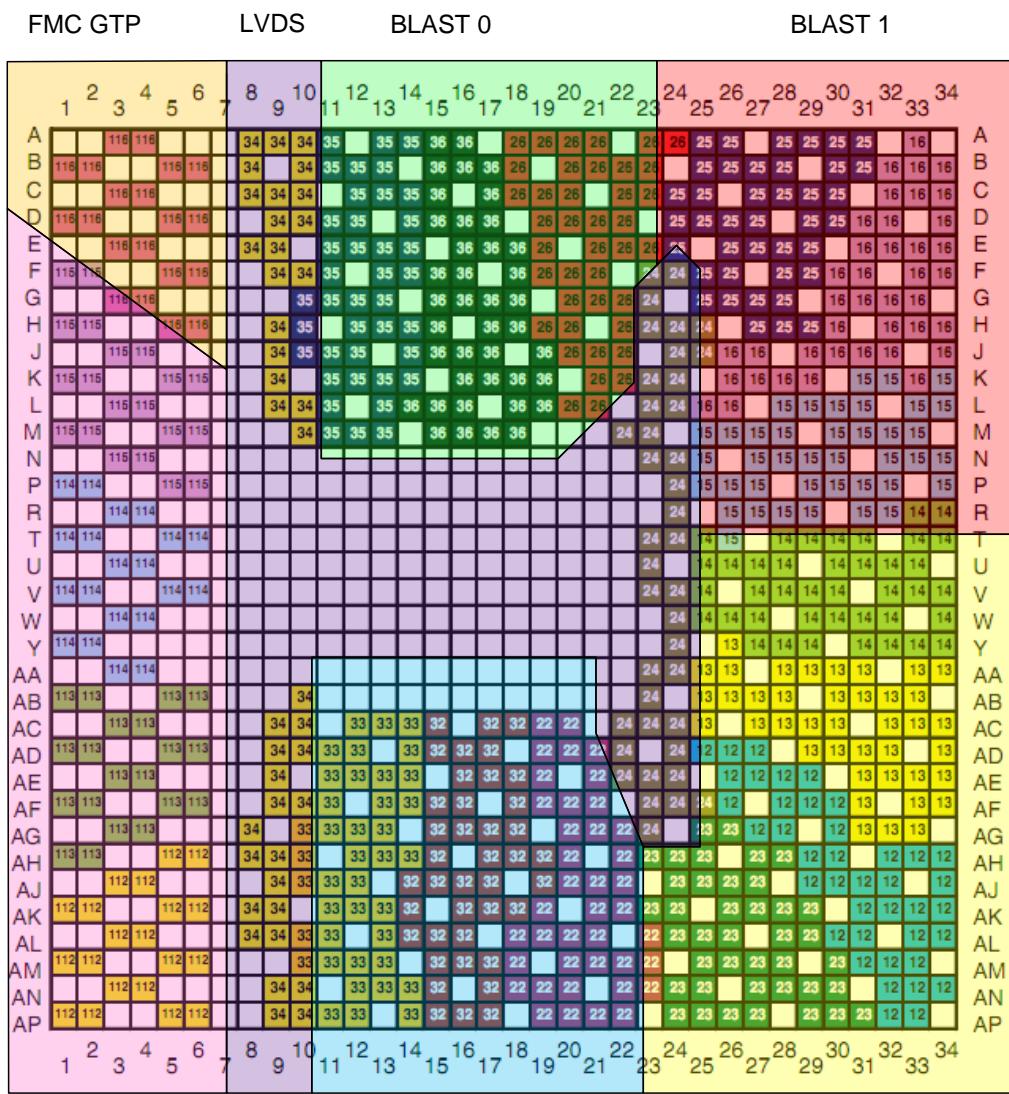
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voltage transients originating from outside the host system which may be introduced through the system.

## 7 Warranty

	Hardware	Software/Firmware
<b>Basic Warranty (included)</b>	1 Year from Date of Shipment	90 Days from Date of Shipment
<b>Extended Warranty (optional)</b>	2 Years from Date of Shipment	1 Year from Date of Shipment

## Appendix A: FPGA Bank Mapping



VPX GTP      LVDS      BLAST 2      FMC

Group	Bank	VCCO	VREF
FMC Bank A	12, 13, 14	VADJ	-
FMC Bank B	23	VIO_B_M2C	-
BLAST 0	26, 35, 36	BLAST0_VIO	0.9V
BLAST 1	15, 16, 25	BLAST0_VIO	0.9V
BLAST 2	22, 32, 33	BLAST2_VIO	0.9V
Miscellaneous	24, 34	2.5V	-

Table 31: FPGA Bank Mapping

Configuration	BLAST 0	BLAST 1	BLAST 2	BLAST0_VIO	BLAST2_VIO
NNN	-	-	-	1.8V	1.8V
ANN	DDR2	-	-	1.8V	1.8V
AAN	DDR2	DDR2	-	1.8V	1.8V
AAA	DDR2	DDR2	DDR2	1.8V	1.8V
BNN	DDR3	-	-	1.5V	1.8V
BBN	DDR3	DDR3	-	1.5V	1.8V
BBB	DDR3	DDR3	DDR3	1.5V	1.5V
QNN	QDR2	-	-	1.8V	1.8V
QQN	QDR2	QDR2	-	1.8V	1.8V
QQQ	QDR2	QDR2	QDR2	1.8V	1.8V
AAQ	DDR2	DDR2	QDR2	1.8V	1.8V
BBQ	DDR3	DDR3	QDR2	1.5V	1.8V
QQA	QDR2	QDR2	DDR2	1.8V	1.8V
QQB	QDR2	QDR2	DDR3	1.8V	1.5V
AAC	DDR2	DDR2	JPEG2000	1.8V	2.5V
BBC	DDR3	DDR3	JPEG2000	1.5V	2.5V
AQC	DDR2	QDR2	JPEG2000	1.8V	2.5V

**Table 32: BLAST VIO Matrix**

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## Appendix B: Errata

### PCB revision 1.0

- SPI FLASH not supported.
- FPGA LED 0 not supported in combination with DDR3 BLAST.
- FPGA LEDs don't go off completely.